■ LSI PIN DESCRIPTION（LSI 端子機能表）

● **AK4385ET** (X6040A00) **DAC** (Digital to Analog Converter) (PSR-S700)

DM: IC400

PIN NO.	NAME	I/O	FUNCTION	PIN NO.	NAME	I/O	FUNCTION
1	MCLK	I	Master Clock	9	AOUTR-	O	Rch Analog out(-)
2	BICK	I	Audio Serial Data Clock	10	AOUTR+	O	Rch Analog out(+)
3	SDTI	I	Audio Serial Date Input	11	AOUTL-	O	Lch Analog out(-)
4	LRCK	I	L/R Clock	12	AOUTL+	O	Lch Analog out(+)
5	PDN	I	Power Down mode	13	Vss	-	Ground
6	CSN	I	Chip Select	14	VDD	-	Power Supply
7	CCLK	I	Control Data Input	15	DZFR	O	Rch Data Zero Input Detect
8	CDTI	I	Control Data Input	16	DZFL	O	Lch Data Zero Input Detect

● **AK4396VF-E2** (X8324A00) **DAC** (Digital to Analog Converter) (PSR-S900)

DM: IC318

PIN NO.	NAME	I/O	FUNCTION	PIN NO.	NAME	I/O	FUNCTION
1	DV_{SS}	-	Digital ground	15	TTL	I	CMOS/TTL level select
2	DV_{DD}	-	Digital power supply +3.3 V	16	VREFL	I	Low level voltage reference input
3	MCLK	I	Master clock input	17	VREFH	I	High level voltage reference input
4	PDN	I	Power-down mode	18	AV_{DD}	-	Analog power supply +5 V
5	BICK	I	Audio serial data clock	19	AV_{SS}	-	Analog ground
6	SDATA	I	Audio serial data input	20	AOUTR-	O	Rch negative analog output
7	LRCK	I	L/R clock	21	AOUTR+	O	Rch positive analog output
8	SMUTE/CSN	I	Soft mute/Chip select	22	AOUTL-	O	Lch negative analog output
9	DFS0/CAD0	I	Sampling speed mode select/Chip address 0	23	AOUTL+	O	Lch positive analog output
10	DEM0/CCLK	I	De-emphasis enable 0/Control data clock	24	VCOM	O	Common voltage output
11	DEM1/CDTI	I	De-emphasis enable 1/Control data input	25	P/S	I	Parallel/serial select
12	DIF0	I	Digital input format	26	TST1/DZFL	O	Test 1/Lch zero input detect
13	DIF1	I		27	TST2/CAD1	I	Test 2/Chip address 1
14	DIF2	I		28	ACKS/DZFR	I/O	Master clock auto setting mode/Rch zero input detect

● HD6417727F160CV (X2890B00) CPU

DM: IC100 (PSR-S700)
DM: IC005 (PSR-S900)

PIN NO.	NAME	I/O	FUNCTION	PIN NO.	NAME	I/O	FUNCTION
1	Vcc-RTC	-	Power supply for RTC (1.9V)	121	PTM[4]/PINT[4]/AFE_RDET_/USB1d_TXDMNS	I	Not in use
2	XTAL2	-	Not in use (XTAL for internal RTC)	122	Reserved/USB1d_SUSPEND	O	
3	EXTAL2	-		123	USB1_ovr_crnt/USBF_VBUS	I	USB function VBUS
4	Vss-RTC	-	Power supply for RTC (0V)	124	USB2_ovr_crnt_	-	USB2_HOST2 over current detection
5	MD1	-	Clock mode setting	125	RTS2_/USB1d_TXENL	O	Not in use
6	MD2	-		126	PTE[2]/USB1_pwr_en	O	USB1 voltage control
7	NMI	-	Not in use (Non-maskable interrupt request)	127	PTE[1]/USB2_pwr_en	O	USB2 voltage control
8	IRQ0/IRL0_/PTH[0]	I	External interrupt request	128	CKE/PTK[5]	O	Enable (SDRAM)
9	IRQ1/IRL1_/PTH[1]	I		129	/RAS3/PTJ[0]	O	RAS for SDRAM
10	IRQ2/IRL2_/PTH[2]	I		130	Reserved/PTJ[1]	O	Not in use
11	IRQ3/IRL3_/PTH[3]	I		131	Reserved//CAS/PTJ[2]	O	CAS for SDRAM
12	IRQ4/PTH[4]	I		132	VssQ	-	VssQ
13	VEPWC	O	VEE control pin for LCD panel	133	Reserved/PTJ[3]	O	Output port (DAC Reset)
14	VCPWC	-	VCC control pin for LCD panel	134	VccQ	-	VccQ
15	MD5	-	Big endian setting	135	Reserved/PTJ[4]	O	Output port (SIO Reset)
16	/BREQ	-	Not in use (bus request)	136	Reserved/PTJ[5]	O	Output port (DAC Mute)
17	/BACK	-	Bus acknowledge	137	Vss	-	Vss
18	VssQ	-	VssQ	138	PTD[5]/CL1	O	LCD line clock
19	CKIO2	-	System clock output	139	Vcc	-	Vcc
20	VccQ	-	VccQ	140	PTD[7]/DON	O	LCD DISPLAY ON
21	D31/PTB[7]	I/O	Data bus	141	PTE[6]/M_DISP	O	LCD alternater
22	D30/PTB[6]	I/O		142	PTE[3]/FLM	O	LCD frame line marker
23	D29/PTB[5]	I/O		143	PTE[0]/TDO	O	JTAG (test data output)
24	D28/PTB[4]	I/O		144	PCC0RESET/DRACK0	O	DMA request acceptance
25	D27/PTB[3]	I/O		145	PCC0DRV_/DACK0_	O	DMA acknowledge
26	D26/PTB[2]	I/O		146	/WAIT	-	Hardware wait request
27	D25/PTB[1]	I/O		147	/RESETM	-	Manual reset request
28	D24/PTB[0]	I/O		148	/ADTRG/PTH[5]	I	Analog A/D trigger
29	VssQ	-	VssQ	149	/IOIS16/PTG[7]	I	Not in use
30	D23/PTA[7]	I/O	Data bus	150	/ASEMD0	-	
31	VccQ	-	VccQ	151	PTG[5]/ASEBRKAK_		
32	D22/PTA[6]	I/O	Data bus	152	PTG[4]	I	
33	D21/PTA[5]	I/O		153	PCC0BVD2/PTG[3]/AUDATA[3]	I	
34	D20/PTA[4]	I/O		154	PCC0BVD1/PTG[2]/AUDATA[2]	I	
35	Vss	-	Vss	155	Vss	-	Vss
36	D19/PTA[3]	I/O	Data bus	156	PCC0CD2/PTG[1]/AUDATA[1]	I	Not in use
37	Vcc	-	Vcc	157	Vcc	-	Vcc
38	D18/PTA[2]	I/O	Data bus	158	PCC0CD1/PTG[0]/AUDATA[0]	I	Not in use
39	D17/PTA[1]	I/O		159	VssQ	-	VssQ
40	D16/PTA[0]	I/O		160	PTF[7]/PINT[15]/TRST_	I	Not in use
41	D15	-	Data bus	161	VccQ	-	VccQ
42	VssQ	-	VssQ	162	PTF[6]/PINT[14]/TMS	I	Not in use
43	D14	-	Data bus	163	PTF[5]/PINT[13]/TDI	I	
44	VccQ	-	VccQ	164	PTF[4]/PINT[12]/TCK	I	
45	D13	-	Data bus	165	PTF[3]/PINT[11]/Reserved	I	
46	D12	-		166	PCCREG_/PTF[2]/Reserved	I	
47	D11	-		167	PCC0VS1_/PTF[1]/Reserved	I	
48	D10	-		168	PCC0VS2_/PTF[0]/Reserved	I	
49	D9	-		169	MD0	-	Clock mode setting
50	D8	-		170	Vcc-PLL1	-	Power supply for Vcc_PLL1 - PLL1(1.9V)
51	D7	-		171	CAP1	-	External capacitance for CAP1 _ PLL1
52	D6	-		172	Vss-PLL1	-	Power supply for Vss_PLL1 _ PLL1(0V)
53	VssQ	-	VssQ	173	Vss-PLL2	-	Power supply for Vss_PLL2 _ PLL2 (0V)
54	D5	-	Data bus	174	CAP2	-	External capacitance for CAP2 _ PLL2
55	VccQ	-	VccQ	175	Vcc-PLL2	-	Power supply for Vcc_PLL2 _ PLL2 (1.9V)
56	D4	-	Data bus	176	PCC0WAIT_/PTH[6]/AUDCK	I	Not in use
57	D3	-		177	Vss	-	Vss
58	D2	-		178	Vcc	-	Vcc
59	D1	-		179	XTAL	-	Clock oscillator
60	D0	-		180	EXTAL	-	External clock
61	A0	-	Address bus	181	LCD15/PTM[3]/PINT[10]	I	Not in use
62	A1	-		182	LCD14/PTM[2]/PINT[9]	I	
63	A2	-		183	LCD13/PTM[1]/PINT[8]	I	
64	VssQ	-	VssQ	184	LCD12/PTM[0]	I	Input port (Flash ROM RY/BY)
65	A3	-	Address bus	185	STATUS0/PTJ[6]	O	Output port (Flash ROM write protect)
66	VccQ	-	VccQ	186	STATUS1/PTJ[7]	O	Output port (Flash ROM ACC)
67	A4	-	Address bus	187	CL2/PTH[7]	O	LCD clock output
68	A5	-		188	VssQ	-	VssQ
69	A6	-		189	CKIO	-	System clock input/output (for SDRAM)
70	A7	-		190	VccQ	-	VccQ
71	A8	-		191	TxD0/SCPT[0]	O	Output port for SCI
72	A9	-		192	SCK0/SCPT[1]	O	Not in use
73	A10	-		193	TxD_SIO/SCPT[2]	O	
74	A11	-		194	SIOMCLK/SCPT[3]	O	
75	VssQ	-	VssQ	195	TxD2/SCPT[4]	O	Output port for SCI
76	A12	-	Address bus	196	SCK_SIO/SCPT[5]	O	Not in use
77	VccQ	-	VccQ	197	SIOFSYNC/SCPT[6]	O	
78	A13	-	Address bus	198	RxD0/SCPT[0]	i	Receiving data 0
79	A14	-		199	RxD_SIO/SCPT[2]	i	Not in use
80	A15	-		200	Vss	-	Vss
81	A16	-		201	RxD2/SCPT[4]	i	Receiving data 2
82	A17	-		202	Vcc	-	Vcc
83	A18	-		203	SCPT[7]/CTS2_/IRQ5	I	Not in use
84	A19	-		204	LCD11/PTC[7]/PINT[3]	O	Output port (PLG CLOCK ON/OFF)
85	A20	-		205	LCD10/PTC[6]/PINT[2]	O	Not in use
86	VssQ	-	VssQ	206	LCD9/PTC[5]/PINT[1]	O	
87	A21	-	Address bus	207	VssQ	-	VssQ
88	VccQ	-	VccQ	208	LCD8/PTC[4]/PINT[0]	O	Not in use
89	A22	-	Address bus	209	VccQ	-	VccQ
90	A23	-		210	LCD7/PTD[3]	O	LCD DATA7
91	Vss	-	Vss	211	LCD6/PTD[2]	O	LCD DATA6
92	A24	-	Address bus	212	LCD5/PTC[3]	O	LCD DATA5
93	Vcc	-	Vcc	213	LCD4/PTC[2]	O	LCD DATA4
94	A25	-	Address bus	214	LCD3/PTC[1]	O	LCD DATA3
95	BS_/PTK[4]	O	Not connected (bus cycle start signal)	215	LCD2/PTC[0]	O	LCD DATA2
96	RD_	-	Read strobe	216	LCD1/PTD[1]	O	LCD DATA1
97	WE0_/DQMLL	O	Write 0 signal	217	LCD0/PTD[0]	O	LCD DATA0
98	WE1_/DQMLU/WE	O	Write 1 signal	218	DREQ0_/PTD[4]	I	DMA request
99	WE2_/DQMUL/ICIORD_/PTK[6]	O	Write 2 signal	219	LCK/UCLK/PTD[6]	I	USB clock
100	VssQ	-	VssQ	220	/RESETP	-	Power on reset request
101	WE3_/DQMUU/ICIOWR_/PTK{7}	O	Write 3 signal	221	CA	-	Hardware standby request
102	VccQ	-	VccQ	222	MD3	-	Bus width setting for area0
103	RD/WR_	O	Read/Write	223	MD4	-	
104	PTE[7]/PCC0RDY/AUDSYNC_	O	I/O	224	/Scan_testen	-	Test pin (fixed to 3.3V)
105	/CS0	-	Chip Select 0	225	Avcc_USB	-	USB analog power supply (3.3V)
106	/CS2	-	Chip Select 2	226	USB1_P	IO	USB1 data input/output (+)
107	/CS3	-	Chip Select 3	227	USB1_M	IO	USB1 data input/output (-)
108	/CS4/PTK[2]	O	Chip Select 4	228	Avss_USB	-	USB analog power supply (0V)
109	/CS5/CE1A_/PTK{3}	O	Chip Select 5	229	USB2_P	IO	USB2 data input/output (+)
110	/CS6/CE1B_	O	Chip Select 6	230	USB2_M	IO	USB2 data input/output (-)
111	CE2A_/PTE[4]	O	Output port (SWP50 Reset)	231	Avcc_USB	-	USB analog power supply (3.3V)
112	CE2B_/PTE[5]	O	Output port (PLG Board Reset)	232	Avss	-	A/D analog power supply (0V)
113	AFE_HC1/USB1d_DPLS/PTK[0]	O	SPD DATA	233	AN[2]/PTL[2]	I	AD converter input
114	AFE_RLYCNT_/USB1d_DMNS/PTK[1]	O	SPD CL	234	AN[3]/PTL[3]	I	
115	VssQ	-	VssQ	235	AN[4]/PTL[4]	I	
116	AFE_SCLK/USB1d_TXDPLS	I	Not in use (USB1 D+ transmission)	236	AN[5]/PTL[5]	I	
117	VccQ	-	VccQ	237	Avcc	-	A/D analog power supply (3.3V)
118	PTM[7]/PTINT[7]/AFE_FS/USB1d_RCV	I	Not in use	238	AN[6]/PTL[6]/DA[1]	I	AD converter input
119	PTM[6]/PTINT[6]/AFE_RXIN/USB1d_SPEED	I		239	AN[7]/PTL[7]/DA[0]	O	DA converter output (LCD contrast)
120	PTM[5]/PTINT[5]/AFE_TXOUT/USB1d_TXSE0	I		240	Avss	-	A/D analog power supply (0V)

● HD6417709SHF200BV (X2687B00) CPU (SH3) (PSR-S900)

DM: IC305

PIN NO.	NAME	I/O	FUNCTION	PIN NO.	NAME	I/O	FUNCTION
1	MD1	I	Mode control	105	CKE/PTK5	I/O	CK enable / Port K
2	MD2	I		106	RAS3L/PTJ0	I/O	RAS address bus / Port J
3	Vcc(RTC)	-	Power supply +1.8 V	107	PTJ1	I/O	Port J
4	XTAL2	O	Crystal oscillator	108	CASL/PTJ2	I/O	CAS address bus / Port J
5	EXTAL2	I		109	VssQ	-	Ground
6	Vss(RTC)	-	Ground	110	CASU/PTJ3	I/O	CAS address bus / Port J
7	NMI	I	Non-maskable interrupt request	111	VccQ	-	Power supply +3.3 V
8	IRQ0/IRL0/PTH0	I	Interrupt request / Port H	112	PTJ4	I/O	Port J
9	IRQ1/IRL1/PTH1	I		113	PTJ5	I/O	
10	IRQ2/IRL2/PTH2	I		114	DACK0/PTD5	I/O	DMA acknowledge / Port D
11	IRQ3/IRL3/PTH3	I		115	DACK1/PTD7	I/O	
12	IRQ4/PTH4	I		116	PTE6	I/O	Port E
13	D31/PTB7	I/O	Data bus / Port B	117	PTE3	I/O	
14	D30/PTB6	I/O		118	RAS3U/PTE2	I/O	RAS address bus / Port E
15	D29/PTB5	I/O		119	PTE1	I/O	Port E
16	D28/PTB4	I/O		120	TDO/PTE0	I/O	Test data / Port E
17	D27/PTB3	I/O		121	BACK	O	Bus acknowledge
18	D26/PTB2	I/O		122	BREQ	I	Bus request
19	VssQ	-	Ground	123	WAIT	I	Hardware wait request
20	D25/PTB1	I/O	Data bus / Port B	124	RESETM	I	Manual reset
21	VccQ	-	Power supply +3.3 V	125	ADTRG/PTH5	I	Analog trigger / Port H
22	D24/PTB0	I/O	Data bus / Port B	126	IOIS16/PTG7	I	Write protect / Port G
23	D23/PTA7	I/O	Data bus / Port A	127	ASEMD0/PTG6	I	ASE mode / Port G
24	D22/PTA6	I/O		128	ASEBRKAK/PTG5	I/O	ASE break acknowledge / Port G
25	D21/PTA5	I/O		129	PTG4/CKIO2	I/O	Port G / Clock output
26	D20/PTA4	I/O		130	AUDATA3/PTG3	I/O	AUD data / Port G
27	Vss	-	Ground	131	AUDATA2/PTG2	I/O	
28	D19/PTA3	I/O	Data bus / Port A	132	Vss	-	Ground
29	Vcc	-	Power supply +1.8 V	133	AUDATA1/PTG1	I/O	AUD data / Port G
30	D18/PTA2	I/O	Data bus / Port A	134	Vcc	-	Power supply +1.8 V
31	D17/PTA1	I/O		135	AUDATA0/PTG0	I/O	AUD data / Port G
32	D16/PTA0	I/O		136	TRST/PTF7/PINT15	I	Test reset / Port F / Port interruption
33	VssQ	-	Ground	137	TMS/PTF6/PINT14	I	Test mode switch / Port F / Port interruption
34	D15	I/O	Data bus	138	TDI/PTF5/PINT13	I	Test data / Port F / Port interruption
35	VccQ	-	Power supply +3.3 V	139	TCK/PTF4/PINT12	I	Test clock / Port F / Port interruption
36	D14	I/O	Data bus	140	IRLS3/PTF3/PINT11	I	Interrupt request / Port F / Port interruption
37	D13	I/O		141	IRL2/PTF2/PINT10	I	
38	D12	I/O		142	IRLS1/PTF1/PINT9	I	
39	D11	I/O		143	IRLS0/PTF0/PINT8	I	
40	D10	I/O		144	MD0	I	Mode control
41	D9	I/O		145	Vcc(PLL1)	-	Power supply +1.8 V
42	D8	I/O		146	CAP1	-	Capacitor
43	D7	I/O		147	Vss(PLL1)	-	Ground
44	D6	I/O		148	Vss(PLL2)	-	Ground
45	VssQ	-	Ground	149	CAP2	-	Capacitor
46	D5	I/O	Data bus	150	VCC(PLL2)	-	Power supply +1.8 V
47	VccQ	-	Power supply +3.3 V	151	AUDCK/PTH6	I	AUD clock / Port H
48	D4	I/O	Data bus	152	Vss	-	Ground
49	D3	I/O		153	Vss	-	
50	D2	I/O		154	Vcc	-	Power supply +1.8 V
51	D1	I/O		155	XTAL1	O	Crystal oscillator
52	D0	I/O		156	EXTAL1	I	
53	A0	O	Address bus	157	STATUS0/PTJ6	I/O	Processor status / Port J
54	A1	O		158	STATUS1/PTJ7	I/O	
55	A2	O		159	TCLK/PTH7	I/O	Timer clock / Port H
56	A3	O		160	/IRQOUT	O	Interrupt request output
57	VssQ	-	Ground	161	VssQ	-	Ground
58	A4	O	Address bus	162	CKIO	I/O	System clock input / output
59	VccQ	-	Power supply +3.3 V	163	VccQ	-	Power supply +3.3 V
60	A5	O	Address bus	164	TXD0/SCPT0	O	Data transmission / SCI port
61	A6	O		165	SCK0/SCPT1	I/O	Serial clock / SCI port
62	A7	O		166	TXD1/SCPT2	O	Data transmission / SCI port
63	A8	O		167	SCK1/SCPT3	I/O	Serial clock / SCI port
64	A9	O		168	TXD2/SCPT4	O	Data transmission / SCI port
65	A10	O		169	SCK2/SCPT5	I/O	Serial clock / SCI port
66	A11	O		170	RTS2/SCPT6	I/O	Transmit request / SCI port
67	A12	O		171	RXD0/SCPT0	I	Data reception / SCI port
68	A13	O		172	RXD1/SCPT2	I	
69	VssQ	-	Ground	173	Vss	-	Ground
70	A14	O	Address bus	174	RXD2/SCPT4	I	Data reception / SCI port
71	VccQ	-	Power supply +3.3 V	175	Vcc	-	Power supply +1.8 V
72	A15	O	Address bus	176	CTS2/IRQ5/SCPT7	I	Transmit clear / Interrupt request / SCI port
73	A16	O		177	MCS7/PTC7/PINT7	I/O	Mask ROM chip select / Port C / Port interruption
74	A17	O		178	MCS6/PTC6/PINT6	I/O	
75	A18	O		179	MCS5/PTC5/PINT5	I/O	
76	A19	O		180	MCS4/PTC4/PINT4	I/O	
77	A20	O		181	VssQ	-	Ground
78	A21	O		182	WAKEUP/PTD3	I/O	Standby mode Interrupt request output / Port D
79	Vss	-	Ground	183	VccQ	-	Power supply +3.3 V
80	A22	O	Address bus	184	RESETOUT/PTD2	I/O	Reset output / Port D
81	Vcc	-	Power supply +1.8 V	185	MCS3/PTC3/PINT3	I/O	Mask ROM chip select / Port C / Port interruption
82	A23	O	Address bus	186	MCS2/PTC2/PINT2	I/O	
83	VssQ	-	Ground	187	MCS1/PTC1/PINT1	I/O	
84	A24	O	Address bus	188	MCS0/PTC0/PINT0	I/O	
85	VccQ	-	Power supply +3.3 V	189	DRAK0/PTD1	I/O	DMA acknowledge / Port D
86	A25	O	Address bus	190	DRAK1/PTD0	I/O	
87	BS/PTK4	I/O	Bus cycle / Port K	191	DREQ0/PTD4	I	DMA request / Port D
88	RD	O	Read strobe	192	DREQ1/PTD6	I	
89	WE0/DQMLL	O	Select signal (D7-D0) / D QM (SDRAM)	193	RESETP	I	Power on reset
90	WE1/DQMLU/WE	O	Select signal (D15-D8) / D QM (SDRAM) / Write enable	194	CA	I	Chip active
91	WE2/DQMUU/ICIORD/PTK6	I/O	Select signal (D23-D16) / D QM (SDRAM) / I/O read / Port K	195	MD3	I	Mode control
92	WE3/DQMUU/ISIOWR/PTK7	I/O	Select signal (D31-D24) / D QM (SDRAM) / I/O write / Port K	196	MD4	I	
93	RD/WR	O	Read / Write	197	MD5	I	
94	AUDSYNC/PTE7	I/O	AUD cycle / Port E	198	AVss	-	Analog ground
95	VssQ	-	Ground	199	AN0/PTL0	I	Analog input / Port L
96	CS0/MCS0	O	Chip select / Mask ROM chip select	200	AN1/PTL1	I	
97	VccQ	-	Power supply +3.3V	201	AN2/PTL2	I	
98	CS2/PTK0	I/O	Chip select / Port K	202	AN3/PTL3	I	
99	CS3/PTK1	I/O		203	AN4/PTL4	I	
100	CS4/PTK2	I/O		204	AN5/PTL5	I	
101	CS5/CE1A/PTK3	I/O	Chip select / Chip enable / Port K	205	AVcc	-	Analog power supply +3.3 V
102	CS6/CE1B	O	Chip select / Chip enable	206	AN6/DA1/PTL6	I/O	Analog input / Analog output / Port L
103	CE2A/PTE4	I/O	Chip enable / Port E	207	AN7/DA0/PTL7	I/O	
104	CE2B/PTE5	I/O		208	AVss	-	Analog ground

• AK5381VT-E2 (X5219A00) ADC (Analog to Digital Converter) (PSR-S900)

DM: IC322

PIN NO.	NAME	I/O	FUNCTION	PIN NO.	NAME	I/O	FUNCTION
1	AINR	I	Rch Analog input pin	9	SDTO	O	Audio serial data output pin
2	AINL	I	Lch Analog input pin	10	LRCK	I/O	Output channel clock pin
3	CKS1	I	Mode select 1 pin	11	MCLK	I	Master clock input pin
4	VCOM	O	Common voltage output pin	12	SCLK	I/O	Audio serial data clock pin
5	AGND	-	Analog ground	13	PDN	I	Power down mode pin
6	VA	-	Analog power supply	14	DIF	I	Audio interface format pin
7	VD	-	Digital power supply	15	CKS2	I	Mode select 2 pin
8	DGND	-	Digital ground	16	CKS0	I	Mode select 0 pin

• S1L50553F21Y000 (X4195A00) GATE ARRAY (PSR-S900)

DM: IC303

PIN NO.	NAME	I/O	FUNCTION	PIN NO.	NAME	I/O	FUNCTION
1	CLKI	I	Clock	41	V_{DD}	-	Power supply
2	CLKO	O		42	RESET	I	Reset
3	V_{DD}	-	Power supply	43	V_{SS}	-	Ground
4	SCANENB	I/O	Scan enable	44	OUT4	O	Output
5	ATPGENB	I/O		45	OUT3	O	
6	V_{SS}	-	Ground	46	INP2	I	Input
7	PLLTEST	I	Test	47	INP1	I	
8	$\overline{\text{PLLRES}}$	I	Reset	48	INP0	I	
9	PLLV_{SS}	-	Ground	49	TESTENB	I/O	Test enable
10	MV$_{DD}$	-	Power supply	50	V_{SS}	-	Ground
11	PLLV_{SS}	-	Ground	51	OSCO		
12	AV$_{DD}$	-	Analog power supply	52	V_{DD}	-	Power supply
13	CHG0			53	OSCI		
14	LPV_{SS}	-	Ground	54	V_{SS}	-	Ground
15	V_{SS}	-		55	SIRQ	I/O	Interrupt request
16	MIRQ	I/O	Interrupt request	56	SCS	I	Control port
17	MCS	I	Control port	57	SWR	I	Write
18	MWR	I	Write	58	SRD	I	Read
19	MRD	I	Read	59	SA		
20	MA			60	V_{SS}	-	Ground
21	V_{DD}	-	Power supply	61	V_{DD}	-	Power supply
22	MD0	I/O	DRAM data bus	62	SD0	I/O	Serial data
23	MD1	I/O		63	SD1	I/O	
24	MD2	I/O		64	SD2	I/O	
25	MD3	I/O		65	SD3	I/O	
26	MD4	I/O		66	SD4	I/O	
27	MD5	I/O		67	SD5	I/O	
28	MD6	I/O		68	SD6	I/O	
29	MD7	I/O		69	SD7	I/O	
30	V_{SS}	-	Ground	70	V_{SS}	-	Ground
31	MD8	I/O	DRAM data bus	71	SD8	I/O	Serial data
32	V_{DD}	-	Power supply	72	V_{DD}	-	Power supply
33	MD9	I/O	DRAM data bus	73	SD9	I/O	Serial data
34	MD10	I/O		74	SD10	I/O	
35	MD11	I/O		75	SD11	I/O	
36	MD12	I/O		76	SD12	I/O	
37	MD13	I/O		77	SD13	I/O	
38	MD14	I/O		78	SD14	I/O	
39	MD15	I/O		79	SD15	I/O	
40	V_{SS}	-	Ground	80	V_{SS}	-	Ground

● DM9000AEP (X7029A00) LAN CONTROLLER

DM: IC300 (PSR-S700)
DM: IC607 (PSR-S900)

PIN NO.	NAME	I/O	FUNCTION	PIN NO.	NAME	I/O	FUNCTION
1	BGRES	I/O	Bandgap pin	25	SD13	I/O	Processor data bus
2	RXVDD25	-	Power output +2.5 V	26	SD12	I/O	
3	RX+	I/O	TP RX input	27	SD11	I/O	
4	RX-	I/O		28	SD10	I/O	
5	RXGND	-	RX ground	29	SD9	I/O	
6	TXGND	-	TX ground	30	VDD	-	Digital power supply +3.3 V
7	TX+	I/O	TP TX output	31	SD8	I/O	Processor data bus
8	TX-	I/O		32	CMD	I	Command type
9	TXVDD25	-	Power output +2.5 V	33	GND	-	Digital ground
10	SD7	I/O	Processor data bus	34	INT	O	Interrupt request
11	SD6	I/O		35	IOR	I	Processor read command
12	SD5	I/O		36	IOW	I	Processor write command
13	SD4	I/O		37	CS	I	Chip select
14	SD3	I/O		38	LED2	O	Link/Active LED
15	GND	-	Digital ground	39	LED1	O	Speed LED
16	SD2	I/O	Processor data bus	40	PWRST	I	Power on reset
17	SD1	I/O		41	TEST	I	Operation mode
18	SD0	I/O		42	VDD	-	Digital power supply +3.3 V
19	EEDIO	I/O	IO data to EEPROM	43	X2	O	Crystal 25 MHz out
20	EECK	O	Clock to EEPROM	44	X1	I	Crystal 25 MHz in
21	EECS	O	Chip select to EEPROM	45	GND	-	Digital ground
22	SD15	I/O	Processor data bus	46	SD	I	Fiber-optic signal detect
23	VDD	-	Digital power supply +3.3 V	47	RXGND	-	RX ground
24	SD14	I/O	Processor data bus	48	BGGND	-	Bandgap ground

● M38044M4-C16FPU0 (X4406100) LED DRIVER/SWITCH SCAN

EIF: IC201

PIN NO.	NAME	I/O	FUNCTION	PIN NO.	NAME	I/O	FUNCTION
1	P62/AN2	I/O	Port6 / A-D converter input	33	P17	I/O	Port1
2	P61/AN1	I/O		34	P16	I/O	
3	P60/AN0	I/O		35	P15	I/O	
4	P57/INT3	I/O	Port5 / Interrupt input	36	P14	I/O	
5	P56/PWM	I/O	Port5 / PWM output	37	P13	I/O	
6	P55/CNTR1	I/O	Port5 / Timer Y	38	P12	I/O	
7	P54/CNTR0	I/O	Port5 / Timer X	39	P11/INT01	I/O	Port1 / Interrupt input
8	P53/SRDY2	I/O	Port5 / Serial ready	40	P10/INT41	I/O	
9	P52/SCLK2	I/O	Port5 / Serial clock	41	P07/AN15	I/O	Port0 / A-D converter input
10	P51/SOUT2	I/O	Port5 / Serial output	42	P06/AN14	I/O	
11	P50/SIN2	I/O	Port5 / Serial input	43	P05/AN13	I/O	
12	P47/SRDY1/CNTR2	I/O	Port4 / Serial ready / Timer Z	44	P04/AN12	I/O	
13	P46/SCLK1	I/O	Port4 / Serial clock	45	P03/AN11	I/O	
14	P45/TxD1	I/O	Port4 / Transmit data	46	P02/AN10	I/O	
15	P44/RxD1	I/O	Port4 / Receive data	47	P01/AN9	I/O	
16	P43/INT2	I/O	Port4 / Interrupt input	48	P00/AN8	I/O	
17	P42/INT1	I/O		49	P37/SRDY3	I/O	Port3 / Serial ready
18	CNVSS	I	Ground	50	P36/SCLK3	I/O	Port3 / Serial clock
19	RESET	I	Reset input	51	P35/TxD3	I/O	Port3 / Transmit data
20	P41/INT00/XCIN	I/O	Port4 / Interrupt input / Sub-clock generating input	52	P34/RxD3	I/O	Port3 / Receive data
21	P40/INT40/XCOUT	I/O	Port4 / Interrupt input / Sub-clock generating output	53	P33/SCL	I/O	Port3 / Serial clock
22	XIN	I	Clock input	54	P32/SDA	I/O	Port3 / Serial data
23	XOUT	O	Clock output	55	P31/DA2	I/O	Port3 / D-A converter output
24	VSS	-	Ground	56	P30/DA1	I/O	
25	P27(LED7)	I/O	Port2	57	VCC	-	Power supply +5V
26	P26(LED6)	I/O		58	VREF	I	Reference voltage
27	P25(LED5)	I/O		59	AVSS	I	Analog ground
28	P24(LED4)	I/O		60	P67/AN7	I/O	Port6 / A-D converter input
29	P23(LED3)	I/O		61	P66/AN6	I/O	
30	P22(LED2)	I/O		62	P65/AN5	I/O	
31	P21(LED1)	I/O		63	P64/AN4	I/O	
32	P20(LED0)	I/O		64	P63/AN3	I/O	

● **T6TZ2XBG-0002** (X7376B00) **SWP51** (Tone Generator)

DM: IC200 (PSR-S700)
DM: IC302 (PSR-S900)

PIN NO.	OUTER NO.	NAME	I/O	FUNCTION
1	E5	VSS	-	Ground
2	D4	VDD1	-	Power supply +1.5 V
3	C3	CD15	I/O	Data bus of internal register
4	B2	CD13	I/O	
5	A1	CD14	I/O	
6	D5	CD6	I/O	
7	E6	CD2	I/O	
8	C4	CD9	I/O	
9	B3	CD11	I/O	
10	A2	CD12	I/O	
11	A3	CD10	I/O	
12	D6	CD1	I/O	
13	E7	VSS	-	Ground
14	C5	CD5	I/O	Data bus of internal register
15	B4	CD8	I/O	
16	A4	CD7	I/O	
17	D7	VSS	-	Ground
18	C6	CD0	I/O	Data bus of internal register
19	E8	VSS	-	Ground
20	D8	VDD3	-	Power supply +3.3 V
21	B5	CD4	I/O	Data bus of internal register
22	A5	CD3	I/O	
23	C7	CA2	I	Address bus of internal regisuter
24	B6	CA0	I	
25	E9	CA8	I	
26	D9	CA9	I	
27	C8	CA5	I	
28	A6	CA1	I	
29	B7	CA3	I	
30	A7	CA4	I	
31	E10	VSS	-	Ground
32	D10	VDD1	-	Power supply +1.5 V
33	C9	CA10	I	Address bus of internal regisuter
34	B8	CA6	I	
35	A8	CA7	I	
36	B9	CA11	I	
37	E11	CA14	I	
38	D11	CA15	I	
39	C10	CA13	I	
40	A9	CA12	I	
41	B10	CSN0	I	Chip select
42	A10	CSN1	I	
43	E12	VSS	-	Ground
44	D12	VDD3	-	Power supply +3.3 V
45	C11	WRN	I	Write strobe
46	B11	RDN	I	Read strobe
47	A11	WAITo	O	Hardware wait request
48	C12	IRQo	O	Interrupt request
49	B12	DREQo	O	DMA request
50	E13	TCK	I	Test pin
51	D13	TRST	I	
52	C13	VSS	-	Ground
53	A12	XO	O	Crystal osc. output
54	B13	XI	I	Crystal osc. input
55	A13	VDD3	-	Power supply +3.3 V
56	A14	SLAVE	I	Master/Slave select
57	E14	TMS	I	Test pin
58	D14	TDO	O	
59	C14	ICN	I	Initial clear
60	B14	RFCLKo	O	PLL Clock
61	B15	PLL_TSTN	I	Test pin
62	C15	PLL_BP	I	
63	D15	VDD3	-	Power supply +3.3 V
64	E15	VSS	-	Ground
65	A15	RFCLKi	I	PLL Clock
66	A16	VDD1	-	Power supply +1.5 V
67	B16	TMODE	I	Test pin
68	C16	PLL_AVD	-	Analog power supply +1.5 V (PLL)
69	D16	NC	-	Not used
70	E16	NC	-	Not used
71	A17	PLL_AVS	-	Analog ground (PLL)
72	B17	TEST1	I	Test pin
73	A18	VSS	-	Ground
74	C17	SYI	I	Sync. clock
75	D17	VDD1	-	Power supply +1.5 V
76	E17	VSS	-	Ground
77	B18	KONTRGo	O	Key on data
78	A19	KONTRGi	I	
79	C18	CK512	O	Master clock (512 Fs)
80	B19	CK128	O	Master clock (256 Fs)
81	D18	BCLK	O	Master clock (64 Fs)
82	E18	SYO	O	Sync. clock
83	C19	HMA20	O	Wave memory address bus
84	A20	HMA21	O	
85	B20	HMA19	O	
86	C20	HMA18	O	
87	D19	VDD3	-	Power supply +3.3 V
88	E19	VSS	-	Ground
89	A21	HMA9	O	Wave memory address bus
90	B21	HMA7	O	
91	A22	HMA6	O	
92	D20	HMA8	O	
93	C21	HMA10	O	
94	E20	HMA17	O	
95	D21	VDD3	-	Power supply +3.3 V
96	B22	HMA11	O	Wave memory address bus
97	A23	HMA4	O	
98	C22	HMA5	O	
99	B23	HMA13	O	
100	E21	VSS	-	Ground
101	D22	HMA12	O	Wave memory address bus
102	C23	HMA3	O	
103	A24	HMA14	O	
104	B24	HMA2	O	
105	A25	HMA1	O	
106	E22	VSS	-	Ground
107	D23	VDD1	-	Power supply +1.5 V
108	C24	HMA15	O	Wave memory address bus
109	B25	HMA16	O	
110	A26	HMA22	O	
111	E23	HMA25	O	
112	F22	VDD3	-	Power supply +3.3 V
113	D24	HMA27	O	Wave memory address bus
114	C25	HMA0	O	
115	B26	HMA23	O	
116	C26	HMA24	O	
117	F23	VDD3	-	Power supply +3.3 V
118	G22	HMA26	O	Wave memory address bus
119	E24	HMA30	O	
120	D25	HMA28	O	
121	D26	HMA29	O	
122	G23	LMA17	O	Wave memory address bus (Lower data memory)
123	F24	LMA19	O	
124	H22	VSS	-	Ground
125	H23	VDD3	-	Power supply +3.3 V
126	E25	LMA20	O	Wave memory address bus (Lower data memory)
127	E26	LMA21	O	
128	G24	LMA9	O	
129	F25	LMA18	O	
130	J22	LMA12	O	
131	J23	LMA4	O	
132	H24	LMA6	O	
133	F26	LMA8	O	
134	G25	LMA7	O	
135	G26	LMA10	O	
136	K22	VSS	-	Ground
137	K23	VDD1	-	Power supply +1.5 V
138	J24	LMA13	O	Wave memory address bus (Lower data memory)
139	H25	LMA11	O	
140	H26	LMA5	O	
141	J25	LMA3	O	
142	L22	LMA16	O	
143	L23	LMA0	O	
144	K24	LMA2	O	
145	J26	LMA14	O	
146	K25	LMA15	O	
147	K26	LMA1	O	
148	M22	VSS	-	Ground
149	M23	VDD3	-	Power supply +3.3 V
150	L24	LMA22	O	Wave memory address bus (Lower data memory)
151	L25	LMA23	O	
152	L26	LMA24	O	
153	M24	LMA27	O	
154	M25	LMA28	O	
155	N22	LMA25	O	
156	N23	LMA26	O	
157	N24	LMA30	O	
158	M26	LMA29	O	
159	N25	MOEN	O	Wave memory output enable
160	N26	MWEN	O	Wave memory write enable
161	P26	LMD15	I/O	Wave memory data bus (Lower 16 bit)
162	P22	VSS	-	Ground
163	P23	VDD3	-	Power supply +3.3 V
164	P24	LMD13	I/O	Wave memory data bus (Lower 16 bit)
165	P25	LMD14	I/O	
166	R25	LMD11	I/O	
167	R24	LMD10	I/O	
168	R23	VDD3	-	Power supply +3.3 V
169	R22	VSS	-	Ground
170	R26	LMD12	I/O	Wave memory data bus (Lower 16 bit)
171	T26	LMD9	I/O	
172	T25	LMD8	I/O	
173	T24	LMD7	I/O	
174	T23	VSS	-	Ground
175	T22	VSS	-	Ground
176	U26	LMD6	I/O	Wave memory data bus (Lower 16 bit)
177	U25	LMD5	I/O	
178	V26	LMD3	I/O	
179	U24	LMD4	I/O	
180	U23	VDD1	-	Power supply +1.5 V
181	U22	VSS	-	Ground
182	V25	LMD2	I/O	Wave memory data bus (Lower 16 bit)
183	W26	LMD0	I/O	
184	V24	LMD1	I/O	
185	W25	DCSL0	O	Wave memory chip select (Low)
186	V23	VDD3	-	Power supply +3.3 V
187	V22	VDD1	-	Power supply +1.5 V
188	W24	DCSL1	O	Wave memory chip select (Low)
189	Y26	DQML3	O	MASK signal
190	Y25	DQML1	O	
191	Y24	DMAL14	O	Address bus (DIMM, SDRAM)
192	W23	VDD3	-	Power supply +3.3 V
193	W22	VSS	-	Ground
194	AA26	DMAL13	O	Address bus (DIMM, SDRAM)
195	AA25	DMAL12	O	
196	AB26	DMAL9	O	
197	Y23	VSS	-	Ground
198	AA24	DMAL11	O	Address bus (DIMM, SDRAM)
199	Y22	VSS	-	Ground
200	AA23	DMAL10	O	Address bus (DIMM, SDRAM)
201	AB25	DMAL8	O	
202	AC26	DMAL6	O	
203	AB24	DMAL7	O	
204	AC25	DMAL5	O	
205	AA22	VSS	-	Ground
206	AB23	VSS	-	Ground
207	AC24	DMAL4	O	Address bus (DIMM, SDRAM)
208	AD26	DMAL3	O	
209	AD25	DMAL2	O	
210	AE26	DMAL0	O	

PIN NO.	OUTER NO.	NAME	I/O	FUNCTION
211	AB22	VSS	-	Ground
212	AC23	VDD1	-	Power supply +1.5 V
213	AD24	DMAL1	O	Address bus (DIMM, SDRAM)
214	AE25	DCSL2	O	Wave memory chip select (Low)
215	AF26	DRAS0	O	DIMM, SDRAM row address strobe (RAS signal)
216	AC22	DCAS0	O	DIMM, SDRAM column address strobe (CAS signal)
217	AB21	VDD3	-	Power supply +3.3 V
218	AD23	DCLKIN	I	DIMM, SDRAM clock input
219	AE24	DQML2	O	MASK signal
220	AF25	DCSL3	O	Wave memory chip select (Low)
221	AF24	DQML0	O	MASK signal
222	AC21	VDD3	-	Power supply +3.3 V
223	AB20	VSS	-	Ground
224	AD22	DWEN0	O	DIMM, SDRAM write enable
225	AE23	DCLK0	O	DIMM, SDRAM clock signal
226	AF23	DCLK1	O	
227	AC20	DCLKE	O	DIMM, SDRAM clock enable
228	AD21	HMD13	I/O	Wave memory data bus (Upper data memory)
229	AB19	VSS	-	Ground
230	AC19	VDD3	-	Power supply +3.3 V
231	AE22	HMD15	I/O	Wave memory data bus (Upper data memory)
232	AF22	HMD14	I/O	
233	AD20	HMD10	I/O	
234	AE21	HMD12	I/O	
235	AB18	VDD1	-	Power supply +1.5 V
236	AC18	VDD3	-	Power supply +3.3 V
237	AD19	HMD7	I/O	Wave memory data bus (Upper data memory)
238	AF21	HMD11	I/O	
239	AE20	HMD9	I/O	
240	AF20	HMD8	I/O	
241	AB17	VSS	-	Ground
242	AC17	VDD1	-	Power supply +1.5 V
243	AD18	HMD4	I/O	Wave memory data bus (Upper data memory)
244	AE19	HMD6	I/O	
245	AF19	HMD5	I/O	
246	AE18	HMD3	I/O	
247	AB16	VSS	-	Ground
248	AC16	VSS	-	Ground
249	AD17	HMD1	I/O	Wave memory data bus (Upper data memory)
250	AF18	HMD2	I/O	
251	AE17	HMD0	I/O	
252	AF17	DCSH0	O	Wave memory chip select (High)
253	AB15	VSS	-	Ground
254	AC15	VDD3	-	Power supply +3.3 V
255	AD16	DCSH1	O	Wave memory chip select (High)
256	AE16	DQMH3	O	MASK signal
257	AF16	DQMH1	O	
258	AD15	DMAH14	O	Address bus (DIMM, SDRAM)
259	AE15	DMAH13	O	
260	AB14	VSS	-	Ground
261	AC14	VSS	-	Ground
262	AD14	DMAH11	O	Address bus (DIMM, SDRAM)
263	AF15	DMAH12	O	
264	AE14	DMAH10	O	
265	AF14	DMAH9	O	
266	AF13	DMAH8	O	
267	AB13	VDD3	-	Power supply +3.3 V
268	AC13	VDD3	-	Power supply +3.3 V
269	AD13	DMAH6	O	Address bus (DIMM, SDRAM)
270	AE13	DMAH7	O	
271	AE12	DMAH4	O	
272	AD12	DMAH3	O	
273	AC12	VDD3	-	Power supply +3.3 V
274	AB12	VSS	-	Ground
275	AF12	DMAH5	O	Address bus (DIMM, SDRAM)
276	AF11	DMAH2	O	
277	AE11	DMAH1	O	
278	AD11	DMAH0	O	
279	AC11	VSS	-	Ground
280	AB11	VSS	-	Ground
281	AF10	DRAS1	O	DIMM, SDRAM row address strobe (RAS signal)
282	AE10	DCSH2	O	Wave memory chip select (High)
283	AF9	DQMH2	O	MASK signal
284	AD10	DCSH3	O	Wave memory chip select (High)
285	AC10	VDD1	-	Power supply +1.5 V
286	AB10	VSS	-	Ground
287	AE9	DQMH0	O	MASK signal
288	AF8	DWEN1	O	DIMM, SDRAM write enable
289	AD9	DCAS1	O	DIMM, SDRAM column address strobe (CAS signal)
290	AE8	DCLK2	O	DIMM, SDRAM clock signal
291	AC9	VDD3	-	Power supply +3.3 V
292	AB9	VDD1	-	Power supply +1.5 V
293	AD8	DCLK3	O	DIMM, SDRAM clock signal
294	AF7	MELO0	O	MEL wave data output
295	AE7	MELO1	O	
296	AD7	MELO2	O	
297	AC8	VDD3	-	Power supply +3.3 V
298	AB8	VSS	-	Ground
299	AF6	MELO3	O	MEL wave data output
300	AE6	MELO4	O	
301	AF5	MELO5	O	
302	AC7	MELO6	O	
303	AD6	MELO7	O	
304	AB7	WCLK0	O	For DAC word clock
305	AC6	WCLK1	O	
306	AE5	EIRQ	O	E bus interrupt request
307	AF4	EICN	O	E bus initial clear
308	AD5	ESDA	I/O	E bus data
309	AE4	ESCL	I/O	E bus clock
310	AB6	MELI0	I	MEL wave data input
311	AC5	MELI1	I	
312	AD4	MELI2	I	
313	AF3	MELI3	I	
314	AE3	MELI4	I	
315	AF2	MELI5	I	
316	AB5	VSS	-	Ground
317	AC4	VDD1	-	Power supply +1.5 V
318	AD3	MELI6	I	MEL wave data input
319	AE2	MELI7	I	
320	AF1	ADLR	O	For ADC word clock
321	AB4	DITo	O	Digital audio output
322	AA5	VSS	-	Ground
323	AC3	AFRM	I/O	Frame signal (ABUS)
324	AD2	ACLK	I/O	Clock signal (ABUS)
325	AE1	ADIR	O	Direction signal (ABUS)
326	AD1	ADAT0	I/O	Data bus (ABUS)
327	AA4	VDD3	-	Power supply +3.3 V
328	Y5	ADAT9	I/O	Data bus (ABUS)
329	AB3	ADAT3	I/O	
330	AC2	ADAT1	I/O	
331	AC1	ADAT2	I/O	
332	Y4	ADAT10	I/O	
333	AA3	ADAT6	I/O	
334	W5	VSS	-	Ground
335	W4	VDD3	-	Power supply +3.3 V
336	AB2	ADAT4	I/O	Data bus (ABUS)
337	AB1	ADAT5	I/O	
338	Y3	ADAT11	I/O	
339	AA2	ADAT7	I/O	
340	V5	ADAT14	I/O	
341	V4	ADAT15	I/O	
342	W3	ADAT13	I/O	
343	AA1	ADAT8	I/O	
344	Y2	ADAT12	I/O	
345	Y1	TDI	I	Test pin
346	U5	VSS	-	Ground
347	U4	VDD1	-	Power supply +1.5 V
348	V3	HRD13	I/O	DRAM data bus
349	W2	HRD15	I/O	
350	W1	HRD14	I/O	
351	V2	HRD12	I/O	
352	T5	HRD7	I/O	
353	T4	HRD6	I/O	
354	U3	HRD10	I/O	
355	V1	HRD11	I/O	
356	U2	HRD9	I/O	
357	U1	HRD8	I/O	
358	R5	VSS	-	Ground
359	R4	VDD3	-	Power supply +3.3 V
360	T3	HRD5	I/O	DRAM data bus
361	T2	HRD4	I/O	
362	T1	HRD3	I/O	
363	R3	HRD2	I/O	
364	R2	HRD1	I/O	
365	P5	VDD3	-	Power supply +3.3 V
366	P4	HRD0	I/O	DRAM data bus
367	P3	RWEN	O	DRAM write enable
368	R1	RQML	O	MASK signal (SDRAM)
369	P2	RCAS	O	DRAM column address strobe (CAS signal)
370	P1	RRAS	O	DRAM row address strobe (RAS signal)
371	N1	RA13	O	DRAM address bus
372	N5	VDD3	-	Power supply +3.3 V
373	N4	VDD3	-	Power supply +3.3 V
374	N3	RA10	O	DRAM address bus
375	N2	RA12	O	
376	M2	RA1	O	
377	M3	RA2	O	
378	M4	VDD3	-	Power supply +3.3 V
379	M5	VSS	-	Ground
380	M1	RA0	O	DRAM address bus
381	L1	RA3	O	
382	L2	RA4	O	
383	L3	RA5	O	
384	L4	VSS	-	Ground
385	L5	VSS	-	Ground
386	K1	RA6	O	DRAM address bus
387	K2	RA7	O	
388	J1	RA9	O	
389	K3	RA8	O	
390	K4	VDD1	-	Power supply +1.5 V
391	K5	VSS	-	Ground
392	J2	RA11	O	DRAM address bus
393	H1	RCLK	O	SDRAM clock signal
394	J3	RCLKE	O	SDRAM clock enable
395	H2	RCLKIN	I	SDRAM, DRAM clock input
396	J4	VDD3	-	Power supply +3.3 V
397	J5	VDD1	-	Power supply +1.5 V
398	H3	RQMH	O	MASK signal (SDRAM)
399	G1	LRD15	I/O	DRAM data bus (Lower data)
400	G2	LRD14	I/O	
401	G3	LRD13	I/O	
402	H4	VDD3	-	Power supply +3.3 V
403	H5	VSS	-	Ground
404	F1	LRD12	I/O	DRAM data bus (Lower data)
405	F2	LRD11	I/O	
406	E1	LRD8	I/O	
407	G4	VDD3	-	Power supply +3.3 V
408	F3	LRD10	I/O	DRAM data bus (Lower data)
409	G5	VDD3	-	Power supply +3.3 V
410	F4	LRD9	I/O	DRAM data bus (Lower data)
411	E2	LRD7	I/O	
412	D1	LRD5	I/O	
413	E3	LRD6	I/O	
414	D2	LRD4	I/O	
415	F5	VSS	-	Ground
416	E4	VSS	-	Ground
417	D3	LRD3	I/O	DRAM data bus (Lower data)
418	C1	LRD2	I/O	
419	C2	LRD1	I/O	
420	B1	LRD0	I/O	

● **YGV628-VZ** (X6356A00) **RGB CONTROLLER AVDP7** (PSR-S900)
● **YGV628B-VZ** (X6356B00) **RGB CONTROLLER AVDP7** (PSR-S900)

DM: IC601

PIN NO.	NAME	I/O	FUNCTION	PIN NO.	NAME	I/O	FUNCTION
1	A23	I	CPU address bus	89	SA13	O	Video memory address bus
2	A22	I		90	VDD	-	Digital power supply +3.3 V
3	A21	I		91	SA11	O	Video memory address bus
4	A20	I		92	SA12	O	
5	VDD	-	Digital power supply +3.3 V	93	SA9	O	
6	A19	I	CPU address bus	94	SA10	O	
7	VSS	-	Digital ground	95	SA8	O	
8	A18	I	CPU address bus	96	SA0	O	
9	A17	I		97	VSS	-	Digital ground
10	A16	I		98	SA1	O	Video memory address bus
11	A15	I		99	SA6	O	
12	A14	I		100	SA7	O	
13	A13	I		101	VDD	-	Digital power supply +3.3 V
14	A12	I		102	SA2	O	Video memory address bus
15	A11	I		103	SA5	O	
16	A10	I		104	SA3	O	
17	A9	I		105	SA4	O	
18	A8	I		106	VSS	-	Digital ground
19	VDD	-	Digital power supply +3.3 V	107	GCK2OUT	O	Dot clock output 2
20	VSS	-	Digital ground	108	VDD	-	Digital power supply +3.3 V
21	A7	I	CPU address bus	109	DRO0	O	Digital R signal output
22	A6	I		110	DRO1	O	
23	A5	I		111	DRO2	O	
24	A4	I		112	DRO3	O	
25	A3	I		113	DRO4	O	
26	A2	I		114	DRO5	O	
27	A1	I		115	DGO0	O	Digital G signal output
28	WRH_N	I	Write strobe input	116	DGO1	O	
29	WRL_N	I		117	VSS	-	Digital ground
30	RD_N	I	Read pulse input	118	DGO2	O	Digital G signal output
31	RESET_N	I	Reset input	119	DGO3	O	
32	VSS	-	Digital ground	120	VDD	-	Digital power supply +3.3 V
33	CS_N	I	Chip select	121	DGO4	O	Digital G signal output
34	VDD	-	Digital power supply +3.3 V	122	DGO5	O	
35	DREQ_N	O	Direct memory access	123	DBO0	O	Digital B signal output
36	INT_N	O	Interrupt	124	DBO1	O	
37	READY_N	O	CPU bus ready	125	DBO2	O	
38	WAIT_N	O	CPU bus wait	126	DBO3	O	
39	D15	I/O	CPU data bus	127	VSS	-	Digital ground
40	D14	I/O		128	DBO4	O	Digital B signal output
41	D13	I/O		129	DBO5	O	
42	D12	I/O		130	YS_N	O	YS signal output
43	VSS	-	Digital ground	131	BLANK_N	O	Non-display interval output
44	D11	I/O	CPU data bus	132	VDD	-	Digital power supply +3.3 V
45	D10	I/O		133	DACVSS	-	DAC analog ground
46	VDD	-	Digital power supply +3.3 V	134	R	O	Analog R signal output
47	D9	I/O	CPU data bus	135	G	O	Analog G signal output
48	D8	I/O		136	B	O	Analog B signal output
49	D7	I/O		137	IREF	-	DAC reference electric-current input
50	D6	I/O		138	DACVDD	-	DAC analog power supply +3.3 V
51	D5	I/O		139	TEST2_N	I	Test pin
52	D4	I/O		140	TEST1_N	I	
53	VSS	-	Digital ground	141	TEST0_N	I	
54	D3	I/O	CPU data bus	142	CSYNC_N	O	Horizontal synchronized signal / Compound synchronized signal output
55	D2	I/O		143	VSYNC_N	O	Vertical synchronized signal output
56	D1	I/O		144	GCK1OUT	O	Dot clock output 1
57	D0	I/O		145	VDD	-	Digital power supply +3.3 V
58	VDD	-	Digital power supply +3.3 V	146	GCK2IN	I	Dot clock input 2
59	SDQ0	I/O	Video memory data bus	147	DRI0	I	Digital R signal input
60	SDQ15	I/O		148	VSS	-	Digital ground
61	VSS	-	Digital ground	149	DRI1	I	Digital R signal input
62	SDQ1	I/O	Video memory data bus	150	DRI2	I	
63	SDQ14	I/O		151	DRI3	I	
64	SDQ2	I/O		152	DRI4	I	
65	SDQ13	I/O		153	DRI5	I	
66	SDQ3	I/O		154	DGI0	I	Digital G signal input
67	VSS	-	Digital ground	155	DGI1	I	
68	SDQ12	I/O	Video memory data bus	156	DGI2	I	
69	VDD	-	Digital power supply +3.3 V	157	DGI3	I	
70	SDQ4	I/O	Video memory data bus	158	VDD	-	Digital power supply +3.3 V
71	SDQ11	I/O		159	DGI4	I	Digital G signal input
72	SDQ5	I/O		160	VSS	-	Digital ground
73	SDQ10	I/O		161	DGI5	I	Digital G signal input
74	VSS	-	Digital ground	162	DBI0	I	Digital B signal input
75	SDQ6	I/O	Video memory data bus	163	DBI1	I	
76	SDQ9	I/O		164	DBI2	I	
77	SDQ7	I/O		165	DBI3	I	
78	SDQ8	I/O		166	DBI4	I	
79	VDD	-	Digital power supply +3.3 V	167	DBI5	I	
80	LDQM	O	Video memory data mask output	168	HSIN_N	I	Horizontal synchronized signal input
81	VSS	-	Digital ground	169	VSIN_N	I	Vertical synchronized signal input
82	WE_N	O	Video memory write enable	170	VDD	-	Digital power supply +3.3 V
83	UDQM	O	Video memory data mask output	171	VSS	-	Digital ground
84	CAS_N	O	Video memory column address strobe output	172	GCK1IN	I	Dot clock input 1
85	SDCKOUT	O	Video memory clock output	173	SYCKIN	I	System clock input
86	RAS_N	O	Video memory low address strobe output	174	PLLVDD	-	PLL analog power supply +3.3 V
87	VSS	-	Digital ground	175	PLLVSS	-	PLL analog ground
88	SCS_N	O	Video memory chip enable	176	FILTER	-	Filter connect pin for PLL

● µPD780031AYGK-N04 (X0031200) LKS

EMKS61A: IC001

PIN NO.	NAME	I/O	FUNCTION	PIN NO.	NAME	I/O	FUNCTION
1	P50/A8	I/O	Port 5 / Higher address bus	33	P10/ANI0	I	Port 1 / A/D converter analog input
2	P51/A9	I/O		34	AVREF	I	A/D converter reference voltage input
3	P52/A10	I/O		35	AVDD	-	Analog power supply
4	P53/A11	I/O		36	RESET	I	System reset input
5	P54/A12	I/O		37	XT2	-	Subsystem clock oscillation
6	P55/A13	I/O		38	XT1	I	
7	P56/A14	I/O		39	IC	-	Internally connected
8	P57/A15	I/O		40	X2	-	Main system clock oscillation
9	Vss0	-	Ground	41	X1	I	
10	VDD0	-	Power supply	42	Vss1	-	Ground
11	P30	I/O	Port 3	43	P00/INTP0	I/O	Port 0 / External interrupt request input
12	P31	I/O		44	P01/INTP1	I/O	
13	P32/SDA0	I/O	Port 3 / Serial data input/output	45	P02/INTP2	I/O	
14	P33/SCL0	I/O	Port 3 / Serial clock input/output	46	P03/INTP3/ADTRG	I/O	Port 0 / External interrupt request input / Trigger signal input
15	P34	I/O	Port 3	47	P70/TI00/TO0	I/O	Port 7 / External count clock input / 16-bit timer/event counter 0 output
16	P35	I/O		48	P71/TI01	I/O	Port 7 / Capture trigger input
17	P36	I/O		49	P72/TI50/TO50	I/O	Port 7 / External count clock input / 8-bit timer/event counter 50 output
18	P20/SI30	I/O	Port 2 / Serial data input	50	P73/TI51/TO51	I/O	Port 7 / External count clock input / 8-bit timer/event counter 51 output
19	P21/SO30	I/O	Port 2 / Serial data output	51	P74/PCL	I/O	Port 7 / Clock output
20	P22/SCK30	I/O	Port 2 / Serial clock input/output	52	P75/BUZ	I/O	Port 7 / Buzzer output
21	P23RxD0	I/O	Port 2 / Serial data input	53	P64/RD	I/O	Port 6 / Strobe signal output for reading
22	P24/TxD0	I/O	Port 2 / Serial data output	54	P65/WR	I/O	Port 6 / Strobe signal output for writing
23	P25/ASCK0	I/O	Port 2 / Serial clock input/output	55	P66/WAIT	I/O	Port 6 / Wait insertion
24	VDD1	-	Power supply	56	P67/ASTB	I/O	Port 6 / Strobe output
25	AVss	-	Ground	57	P40/AD0	I/O	Port 4 / Lower address/data bus
26	P17/ANI7	I	Port 1 / A/D converter analog input	58	P41/AD1	I/O	
27	P16/ANI6	I		59	P42/AD2	I/O	
28	P15/ANI5	I		60	P43/AD3	I/O	
29	P14/ANI4	I		61	P44/AD4	I/O	
30	P13/ANI3	I		62	P45/AD5	I/O	
31	P12/ANI2	I		63	P46/AD6	I/O	
32	P11/ANI1	I		64	A47/AD7	I/O	

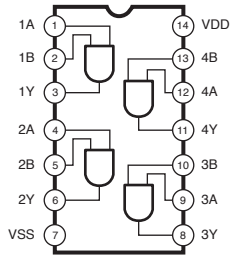
● MB3516APF-G-BND-EF (X2314A00) RGB ENCODER (PSR-S900)

DM: IC606

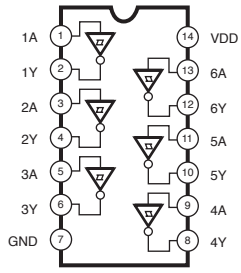
PIN NO.	NAME	I/O	FUNCTION	PIN NO.	NAME	I/O	FUNCTION
1	GND1	-	Ground	13	N.C.	-	Not used
2	R-IN	I	Analog R signal input	14	N.C.	-	Not used
3	G-IN	I	Analog G signal input	15	CROMA-OUT	O	Chrominance signal output
4	B-IN	I	Analog B signal input	16	Y-OUT	O	Y-signal output
5	N.C.	-	Not used	17	Y-TRAP	-	Luminance signal band control
6	fsc-IN	I	Subcarrier input	18	N.C.	-	Not used
7	NTSC/PAL-IN	I	NTSC/PAL selector	19	Vcc2	-	Power supply +5 V
8	N.C.	-	Not used	20	VIDEO-OUT	O	Composite video signal output
9	N.C.	-	Not used	21	B-OUT	O	Analog B signal output
10	CSYNC-IN	I	Composite sync signal input	22	G-OUT	O	Analog G signal output
11	N.C.	-	Not used	23	R-OUT	O	Analog R signal output
12	Vcc1	-	Power supply +5 V	24	GND2	-	Ground

■ IC BLOCK DIAGRAM（IC ブロック図）

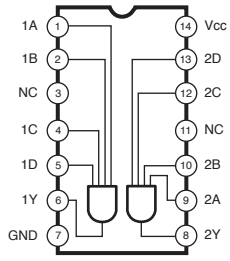
● **SN74AHC08PWR** (X2713A00)
Quad 2 Input AND
DM: IC029 (PSR-S900)



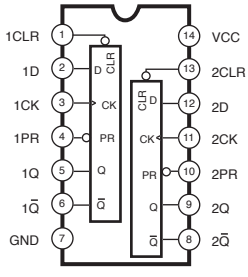
● **SN74AHC14PWR** (X3098A00)
Hex Inverter
DM: IC011 (PSR-S700)
DM: IC004, 010 (PSR-S900)



● **HD74LV21ATELL** (X0010A00)
● **SN74LV21APWR** (X2377A00)
Dual 4 Input AND
DM: IC908 (PSR-S700)
DM: IC021 (PSR-S900)

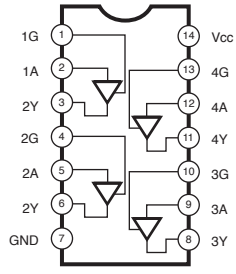


● **TC74ACT74FT(EL)** (X6536A00)
DM: IC603 (PSR-S900)
● **TC74VHC74FT(EL,K)** (XV892B00)
DM: IC309 (PSR-S900)
Dual D-Type Flip-Flop

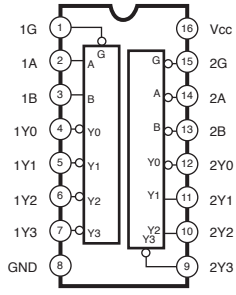


INPUTS				OUTPUTS	
PR	CLR	CLK	D	Q	Q
L	H	X	X	H	L
H	L	X	X	L	H
L	L	X	X	H	H
H	H	f	H	H	L
H	H	f	L	L	H
H	H	L	X	Q₀	Q₀

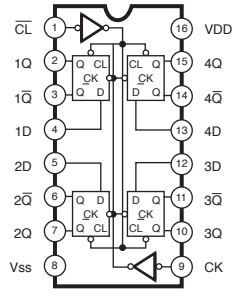
● **HD74LV126ATELL** (X3123A00)
● **SN74LV126APWR** (X3865A00)
● **TC74VHC126FT(EL,K)** (X2891B00)
Bus Buffer
DM: IC003 (PSR-S900)



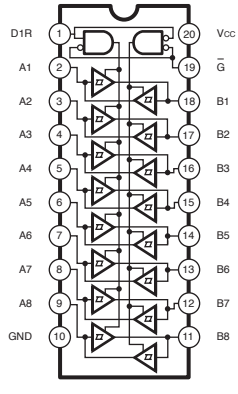
● **SN74LV139APWR** (X7618A00)
DM: IC900 (PSR-S700)
● **TC74VHC139FT** (XV893A00)
DM: IC028 (PSR-S900)
Dual 2 to 4 Demultiplexer



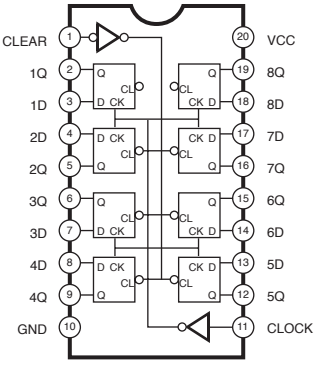
● **SN74LV175APWR** (X5535A00)
Quad D-Type Flip-Flop
DM: IC907 (PSR-S700)



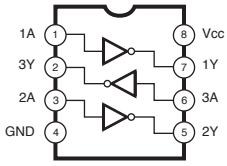
● **HD74LV245ATELL-E** (XW744A00)
● **SN74LV245APWR** (X3693A00)
● **TC74VHC245FT(EL,K)** (XU797B00)
Octal 3-State Bus Transceiver
DM: IC901-904 (PSR-S700)
DM: IC017-020, 023, 024 (PSR-S900)



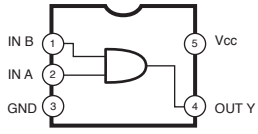
● **HD74LV273ATELL** (X2689A00)
● **SN74LV273APWR** (X5074A00)
Octal D-Type Flir Flop
DM: IC027 (PSR-S900)



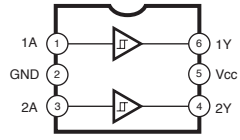
● **TC7WHU04FU** (X4063A00)
Triple Inverter
DM: IC310, 311, 600, 602 (PSR-S900)



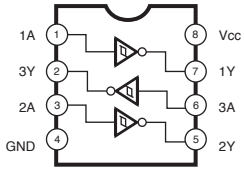
● **TC7SH08FU** (XR680A00)
2 Input AND Gate
DM: IC307 (PSR-S900)



● **SN74LVC2G17DCKR** (X4454A00)
Dual Schmitt-trigger Buffer
DM: IC070 (PSR-S700)

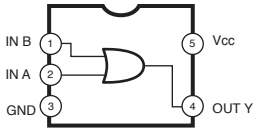


● **TC7W14FU** (XN883A00)
Triple Inverter
DM: IC328 (PSR-S900)

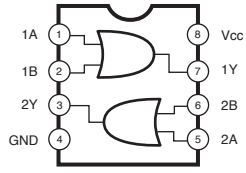


● **TC7SET32FU** (XW814A00)
DM: IC009 (PSR-S900)

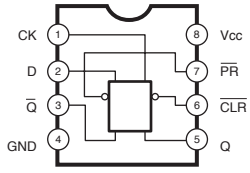
● **TC7SH32FU** (XW633A00)
DM: IC030 (PSR-S900)
2-Input OR Gate



● **TC7W32FU** (XQ173A00)
Dual 2 Input OR Gate
DM: IC905 (PSR-S700)

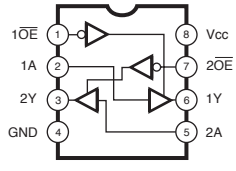


● **TC7WH74FU** (XS680A00)
D-Type flip-Flop
DM: IC308 (PSR-S900)

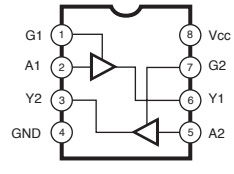


INPUTS				OUTPUTS		FUNCTION
$\overline{CLR}$	$\overline{PR}$	D	CK	Q	$\overline{Q}$	
L	H	X	X	L	H	CLEAR
H	L	X	X	H	L	PRESET
L	L	X	X	H	H	—
H	H	L	⎍	L	H	—
H	H	H	⎍	H	L	—
H	H	X	⎏	Qn	$\overline{Q}$n	NO CHANGE

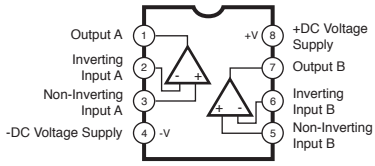
● **SN74LVC2G125DCUR** (X7171A00)
Dual Bus Buffer Gate
DM: IC031 (PSR-S700)



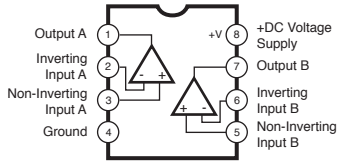
● **TC7WT126FU** (X7703A00)
Dual Bus Buffer
DM: IC604 (PSR-S900)



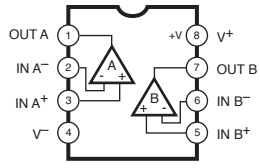
- **NJM2068M-D(TE2)** (X3505A00)
  DM: IC420, 490 (PSR-S700)
  DM: IC316, 324, 325 (PSR-S900)
- **NJM4556AM-TE1** (X5049A00)
  AM: IC048
- **µPC4570G2-E1-A** (X7351A00)
  AM: IC013, 050, 055, 093 (PSR-S700)
  AM: IC013, 050, 055, 064, 093 (PSR-S900)
  Dual Operational Amplifier



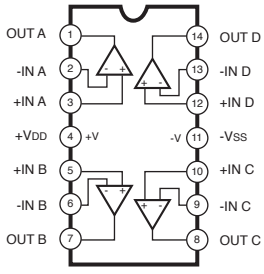
- **NE5532DR** (X5482A00)
  AM: IC013, 050, 055, 093 (PSR-S700)
  AM: IC013, 050, 055, 064, 093 (PSR-S900)
  DM: IC420, 490 (PSR-S700)
  DM: IC316, 324, 325 (PSR-S900)
- **NJM12904V(TE1)** (X3836A00)
  PNCA: IC001 (PSR-S900)
  Dual Operational Amplifier



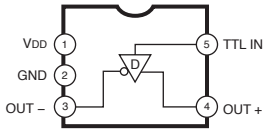
- **LMV358AM8X-NL** (X7287A00)
  Dual Operational Amplifier
  EIF: IC202



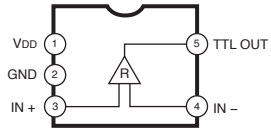
- **µPC4574G2-E1-A** (X7391A00)
  Quad Operational Amplifier
  AM: IC021, 022, 031, 032, 043



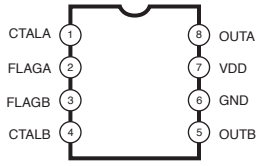
- **DS90LV011ATMF/NOPB** (X6788A00)
  3V LVDS Single High Speed Differential Driver
  DM: IC050 (PSR-S700)
  DM: IC012 (PSR-S900)



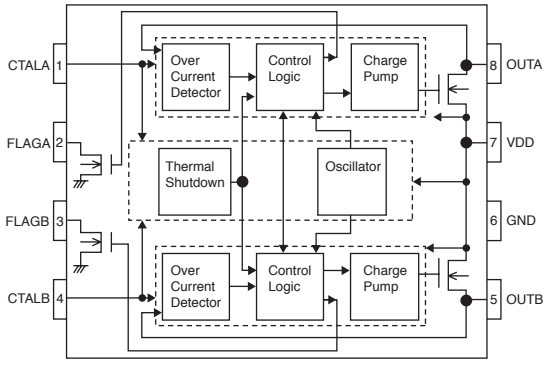
- **DS90LV012ATMF/NOPB** (X6789A00)
  3V LVDS Single CMOS Differential Line Receiver
  EIF: IC204



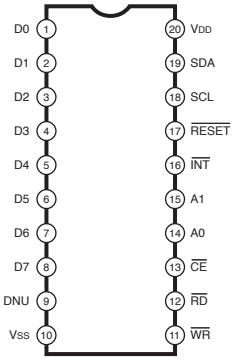
- **BD6516F-E2** (X7950A00)
  High Side Switch
  DM: IC030 (PSR-S700)
  DM: IC002 (PSR-S900)

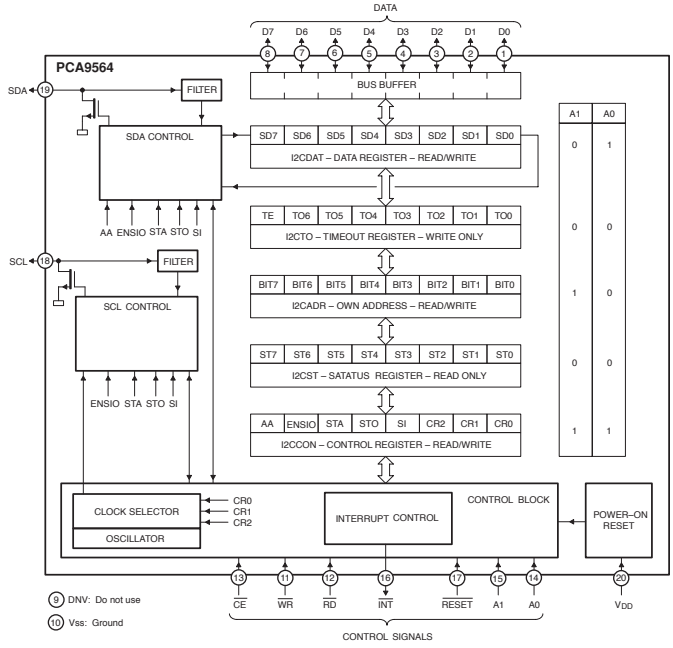


Pin No.	Pin Name	Pin Function
1 4	CTRLA CTRLB	Control input
2 3	FLAGA FLAGB	Error flag output
5 8	OUTB OUTA	Switch output
6	GND	Ground
7	VDD	Switch input



- **PCA9564PW** (X6155A00)
  Parallel bus to I²C-bus controller
  DM: IC026 (PSR-S900)





- **LA4705NA-E** (XQ619A00)
  Power Amplifier
  AM: IC051